USB5953
User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

USB5953 data acquisition board is compatible with USB bus, may access the computer via USB cable, which constitutes the laboratory, product quality testing center, field monitoring and control, medical equipment and other fields' data acquisition, waveform analysis and processing system, it can also constitute the industrial production process control monitoring system. And it has a small size, plug-and-play characteristics, so it is the best choice for portable system.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- USB5953 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Analog Input

- Converter Type: AD7663ASTZ (default AD7663, can also use AD7665)
- Input Range: ±10V, ±5V (default), ±2.5, 0~10V, 0~5V
- 16-bit resolution
- Sample Rate: 31Hz~250KS/s (AD7665, sample rate: 31Hz~500KHz)

Note: The actual channel sampling rate = sampling rate / number of sampling channels
Frequency Formula: sampling frequency= main frequency/the number of frequency division, main frequency = 40MHz, 32-bit frequency division, the number of frequency division range: 160~1290322 (when use AD7665, the number of frequency division range: 80~1290322).

- Number of Channels: 14SE/6DI
- Data Read Mode: non-empty and half-full query mode
- FIFO Size: 8K
- Memory Flag: non-empty and half-full
- AD Mode: continuum sampling, grouping sampling
- Group Interval: software-configurable, minimum value is sampling period, maximum value is 32767us
- Loops of Group: software-configurable, minimum value is one time , maximum value is 255 times
- Clock Source: external clock, internal clock (software-configurable)
- Trigger Mode: software trigger, hardware trigger (external trigger)
- Trigger Type: level trigger, edge trigger
- Trigger Direction: negative, positive, either positive or negative trigger
- Trigger Source: ATR, DTR
- ATR Input Range: 0~10V
- DTR Input Range: TTL Level

- Analog Input impedance: 10 MΩ
- Programmable amplifier type: AD8251(default), compatible AD8250, AD8253
- Amplifier Set-up Time: 785ns(0.001%)(max)
- AD Conversion Time: 1.25μs
- Non-linear error: ±3LSB(Max)
- System Measurement Accuracy: 0.01%
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: −20℃~70℃

Analog Output

- Converter Type: AD5725
- Output Range: ±10V, ±5V(default), 0~10V, 0~5V
- 12-bit resolution
- Set-up Time: 10μs (0.01%)
- Channel No.: 4-channel
- Non-linear error: ±1LSB (Max)
- Output Error (full-scale): ±1LSB
- Operating Temperature Range: 0℃～+50℃
- Storage Temperature Range: -20℃～+70℃

Digital Input

- Channel No.: 6-channel
- Electric Standard: TTL compatible
- High Level: ≧2V
- Low Level: ≦0.8V

Digital Output

- Channel No.: 6-channel
- Electrical Standard: TTL compatible
- High Level: ≧3.8V
- Low Level: ≦0.44V
- Power-on output: low level

CNT Counter/timer

- 1-ch 32-bit down counter/timer
- Count Mode: 6 mode (software-configurable)
- Input and Output Electrical Standard: TTL level
- Clock Source (CLK0):1Hz~10MHz
- Gate (GATE0): rising edge, high level, low level
- Counter Output (OUT0): high level, low level

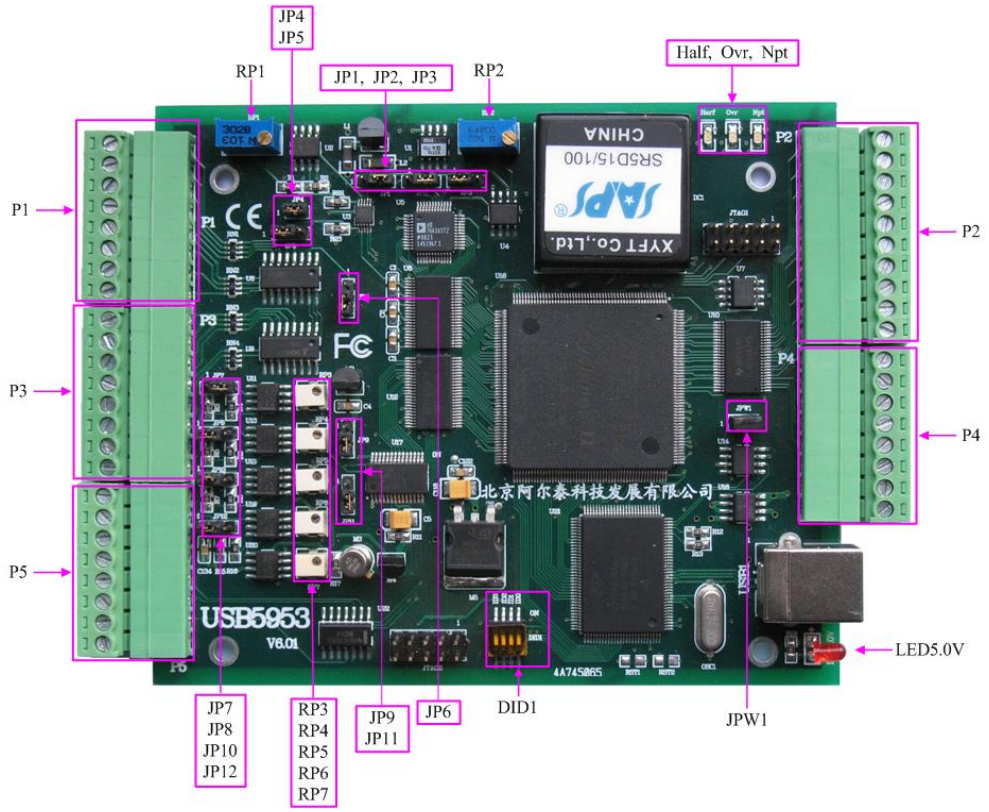
Other Features

Board Clock Oscillation: 40MHz

Board Dimension: 116mm (L) * 98.7mm (W) * 16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Components Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

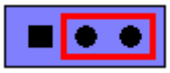
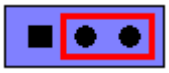
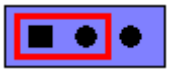
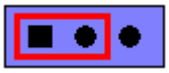
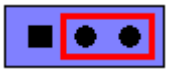
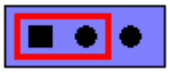
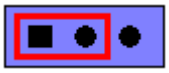
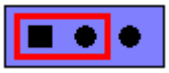
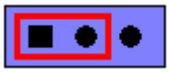
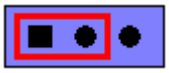
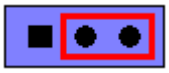
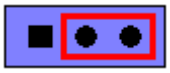
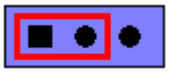
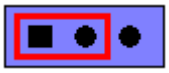
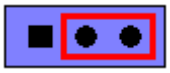
P1, P3, and P5: analog signal, trigger signal and clock signal input/output ports
P2, P4: digital signal input/output and counter input/output ports

2.2.2 Potentiometer

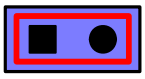
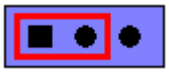
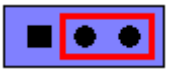
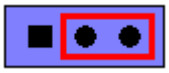
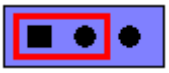
RP1: Analog signal input zero-point adjustment potentiometer
RP2: Analog signal input full-scale adjustment potentiometer
RP7: AO0~AO3 zero-point adjustment potentiometer
RP3: AO0 full-scale adjustment potentiometer
RP4: AO1 full-scale adjustment potentiometer
RP5: AO2 full-scale adjustment potentiometer
RP6: AO3 full-scale adjustment potentiometer

2.2.3 Jumper

JP1, JP2, and JP3: analog input range selection

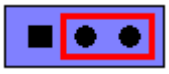
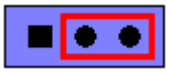
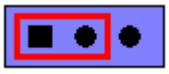
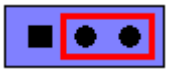
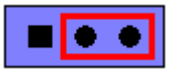
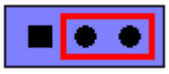
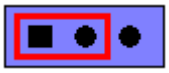
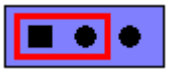
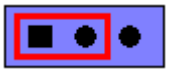
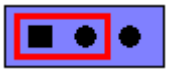
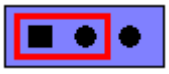
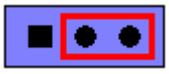
Input Range	JP1	JP2	JP3
±10V			
±5V			
±2.5V			
0~10V			
0~5V			

JP4, JP5, and JP6: analog input single-end or differential selection

Input Mode	JP4	JP5	JP6
SE			
DI			

JP9, JP11: AO0~AO3 unipolar, bipolar selection

JP7, JP8, JP10, and JP12: AO0~AO3 range selection

Range	JP9	JP11	JP7(AO0) JP8(AO1) JP10(AO2) JP12(AO3)
0~5V			
0~10V			
±5V			
±10V			

JPW1: load USB program, 1-2 shorted (default)

2.2.4 Status indicator

Half: FIFO half-full indicator, on for normal condition.

Ovr: FIFO overflow indicator, on for normal condition.

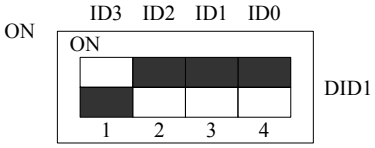
Npt: FIFO non-empty indicator, on for normal condition.

LED5.0V: 5.0V power supply indicator, on for normal condition.

2.2.5 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one USB5953 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-place numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: place "ID3" is the high bit."ID0" is the low bit, and the black part in the diagram represents the location of the switch. (Test software of the company often uses the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible.).

The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

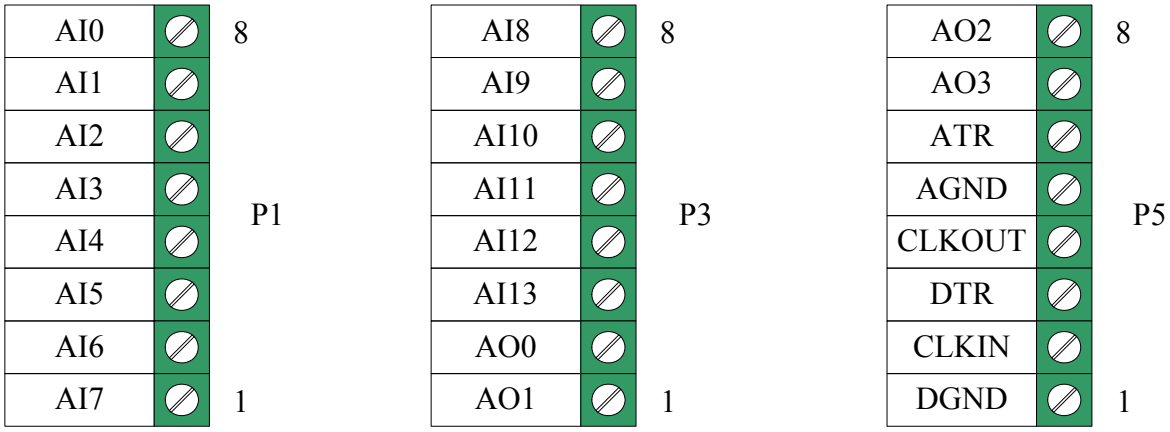
The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

Chapter 3 Signal Port

3.1 The Definition of Signal Input Ports

Pin definition of P1, P3, and P5

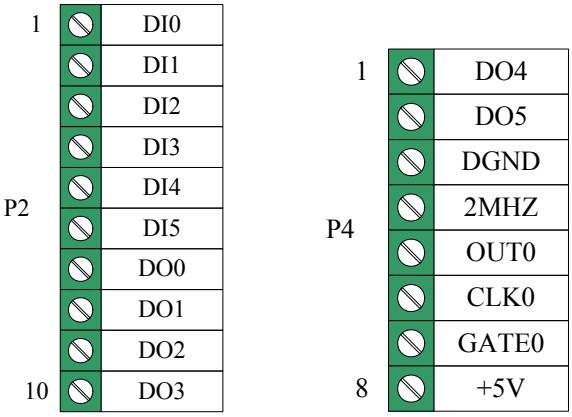


Pin definition about analog inputs

Pin name	Pin feature	Pin function definition
AI0~AI13	Input	Analog input
AO0~AO3	Output	Analog output
ATR	Input	Analog trigger
AGND	GND	Analog ground
CLKIN	Input	External clock input
CLKOUT	Output	Internal clock output
DTR	Input	Digital trigger
DGND	GND	Digital ground

3.2 The Definition of Digital Signal Ports

Pin definition of P2, P4



Pin definition

Pin name	Type	Pin function definition
DI0~DI5	Input	Digital input.
DO0~DO5	Output	Digital output.
2MHZ	Output	On-board 2MHz clock oscillator pulse output, output cycle 0.5 microseconds.
CLK0	Input	Timer/counter clock source input.
GATE0	Input	Timer/counter gate input, reference ground is DGND.
OUT0	Output	Timer/Counter output, the default is counter output.
DGND	GND	Digital ground.

Chapter 4 Connection Ways for Each Signal

4.1 Analog Input Connection Mode

4.1.1 Single-ended Input Connection Mode

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

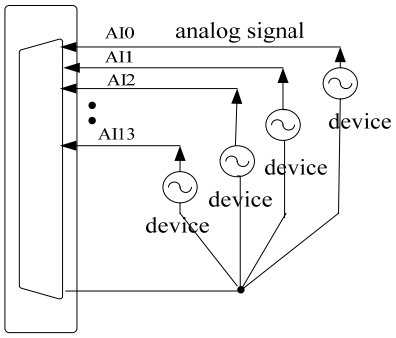


Figure 4.1 single-ended input connection

4.1.2 Double-ended Input Connection Mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB5953 software manual.

According to the diagram below, USB5953 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 7-channel analog input signal is connected to AI0~AI6, the negative side of the analog input signal is connected to AI7~AI13, equipments in industrial sites share the AGND with USB5953 board.

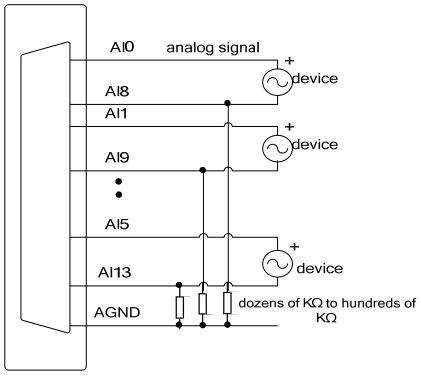


Figure 4.2 double-ended input connection

4.2 Other connections

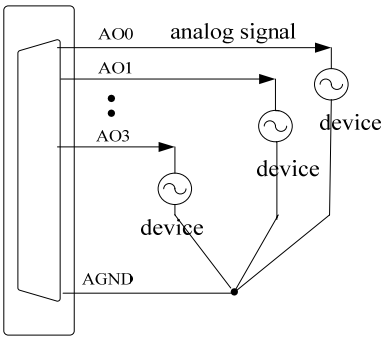


Figure 4.3 analog signal output connection

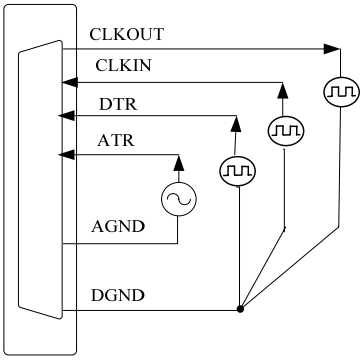


Figure 4.5 Clock Input/Output and Trigger Signal Connection

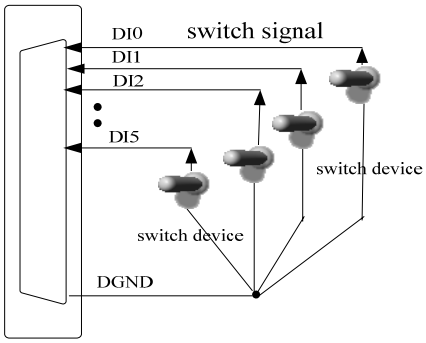


Figure 4.4 digital signal input connection

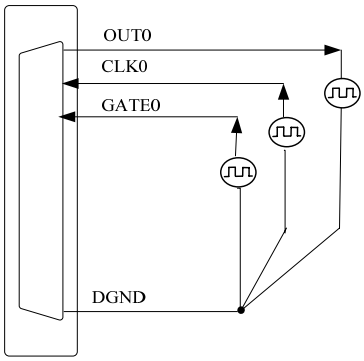


Figure 4.6 Timer/Counter signal connection

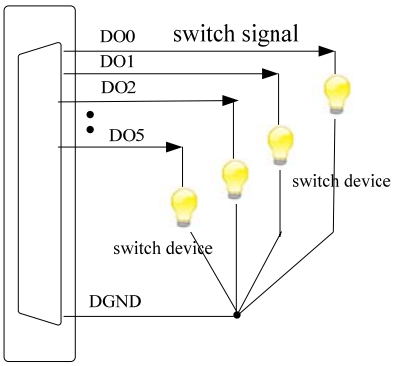


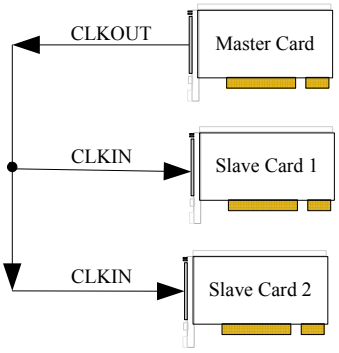
Figure 4.5 digital signal output connection

4.3 Methods of Realizing the Multi-card Synchronization

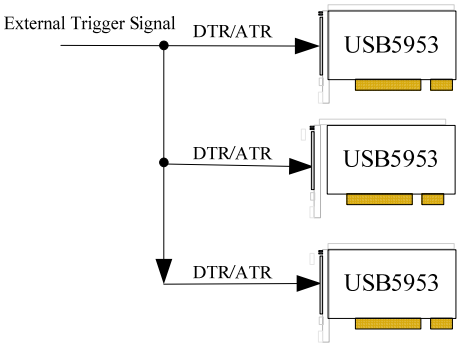
Three methods can realize the synchronization for the USB5953, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could

consider using the multi-card cascaded model to expand the number of channels.

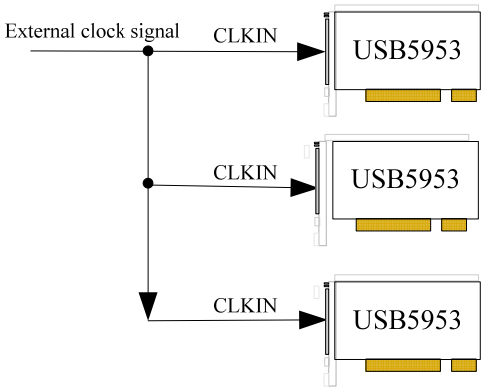


When using the common external trigger, please make sure all parameters of different USB5953 are the same. At first, configure hardware parameters, and use digital signal triggering (DTR), then connect the sampled signal, input triggering signal from DTR pin, then click “Start” button, at this time, USB5953 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



Note: when using the DTR, select the internal clock mode

When using the common external clock trigger, please make sure all parameters of different USB5953 are the same. At first, configure hardware parameters, and use external clock, then connect the sampled signal, then click “Start” button, at this time, USB5953 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:



Chapter 5 The Instruction of the Trigger Function

5.1 Internal Trigger Mode

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = USB5953_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the InitDeviceAD function, it will generate AD start pulse, AD immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the AD work pulse is decided by the sampling frequency.

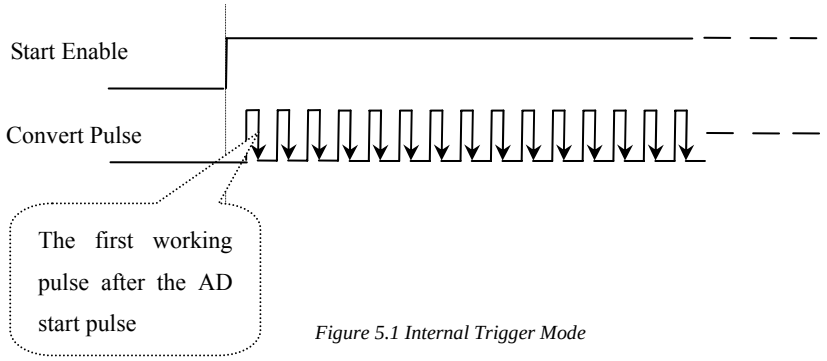


Figure 5.1 Internal Trigger Mode

5.2 External Trigger Mode

(一) ART

When AD is in the initialization, if the AD hardware parameter ADPara.TriggerMode = USB5953_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the InitDeviceAD function, AD will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source is ATR (Analog Trigger Source). AO0 supports the trigger level.

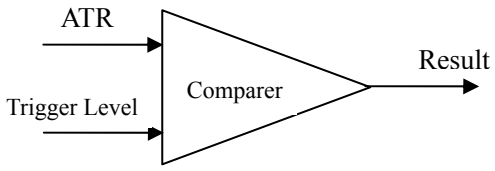


Figure 5.2 Analog compare

The trigger modes include the edge trigger and level trigger.

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger AD conversion. When TriggerType=USB5953_TRIGTYPE_EDGE, it is the edge trigger type.
When ADPara.TriggerDir = USB5953_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the ATR trigger signal is on the falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

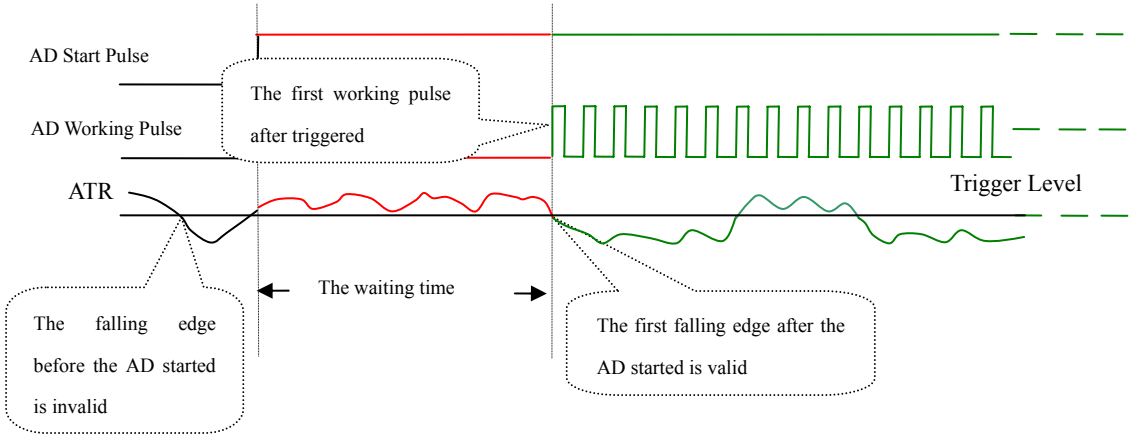


Figure 5.3 Falling edge Trigger

When ADPara.TriggerDir = USB5953_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the ATR trigger signal is on the rising edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition.

When ADPara.TriggerDir = USB5953_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the ATR trigger signal is on the rising or falling edge, AD will immediately access to the conversion process, and its follow-up changes have no effect on AD acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）Triggering level function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger AD conversion. When ADPara.TriggerType = USB5953_TRIGTYPE_PULSE, it is level trigger type.
When ADPara.TriggerDir = USB5953_TRIGDIR_NEGATIVE, AD is in the conversion process if the ATR is lower than the trigger level. And AD conversion will automatically stop if the ATR is higher than the trigger level. AD's work status changes with changes of ATR.

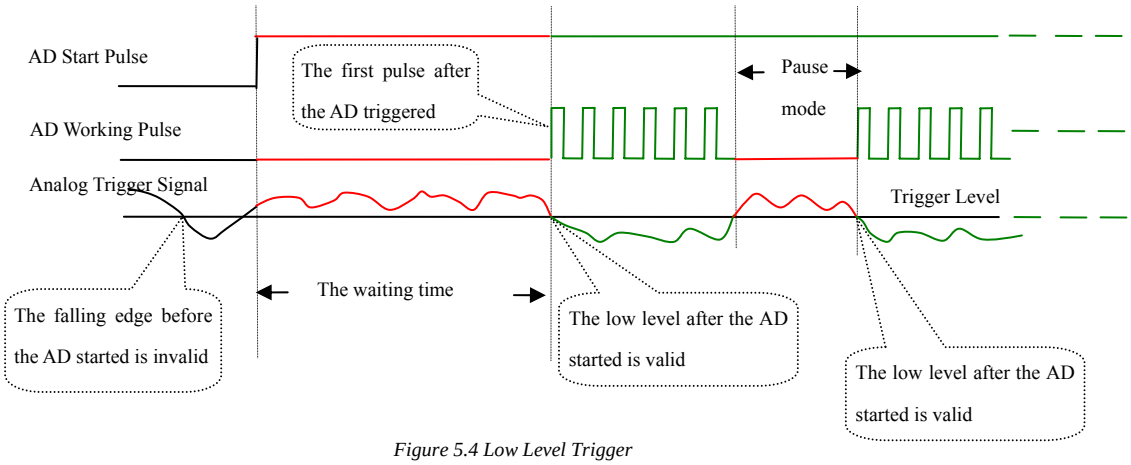


Figure 5.4 Low Level Trigger

When ADPara.TriggerDir = USB5953_TRIGDIR_POSITIVE, AD is in the conversion process if the ATR is higher than the trigger level. And AD conversion will automatically stop if the ATR is lower than the trigger level. AD's work status changes with changes of ATR.

When ADPara.TriggerDir = USB5953_TRIGDIR_POSIT_NEGAT, it means the trigger level is low. The effect is the same as the internal software trigger.

(二) DTR

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger A/D conversion.

When ADPara.TriggerDir = USB5953_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the DTR trigger signal is on the falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

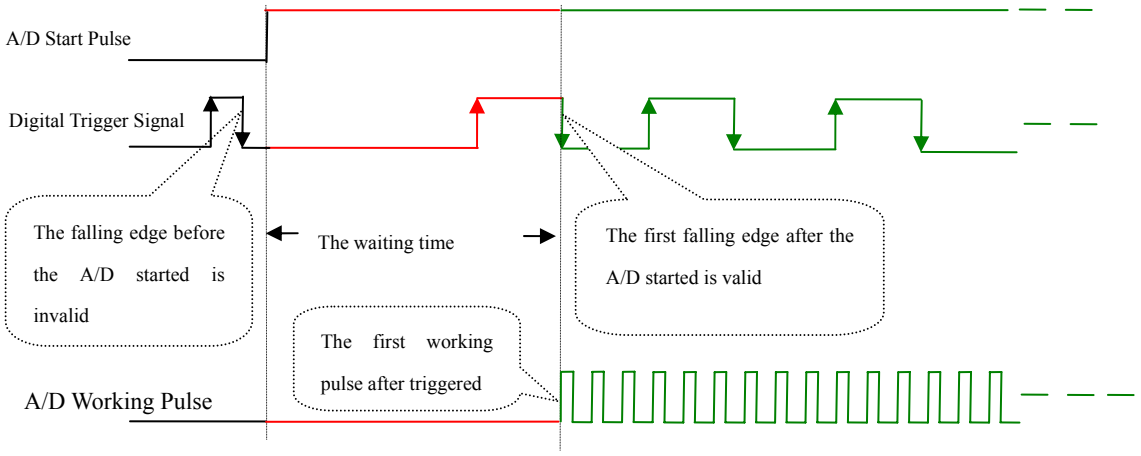


Figure 5.5 Falling edge Trigger

When ADPara.TriggerDir = USB5953_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the DTR trigger signal is on the rising edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

When ADPara.TriggerDir = USB5953_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the DTR trigger signal is on the rising or falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）Level trigger function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger A/D conversion.

When ADPara.TriggerDir = USB5953_TRIGDIR_NEGATIVE, it means the trigger level is low. When DTR trigger signal is in low level, A/D is in the conversion process, once the trigger signal is in the high level, A/D conversion will automatically stop, when the trigger signal is in the low level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the low level.

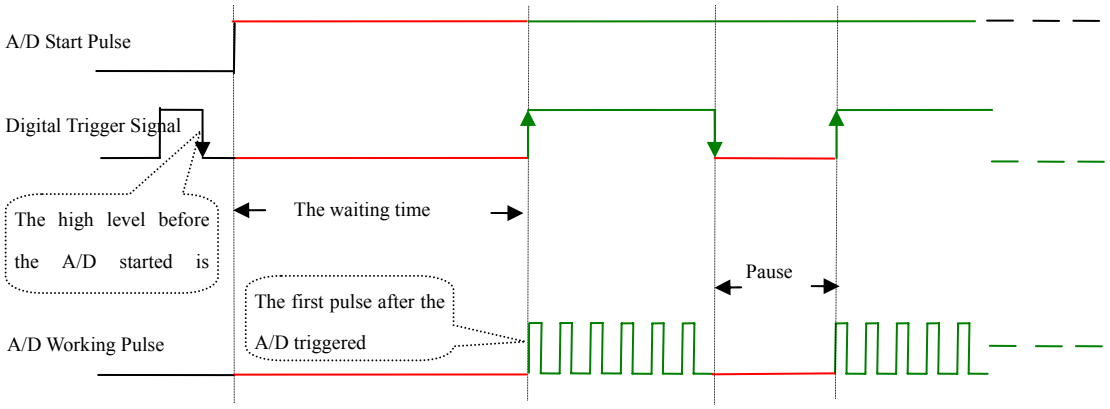


Figure 5.6 High Level Trigger

When ADPara.TriggerDir = USB5953_TRIGDIR_POSITIVE, it means the trigger level is high. When DTR trigger signal is in high level, A/D is in the conversion process, once the trigger signal is in the low level, A/D conversion will automatically stop, when the trigger signal is in the high level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.

When ADPara.TriggerDir = USB5953_TRIGDIR_POSIT_NEGAT, it means the trigger level is low or high. The effect is the same as the internal software trigger.

Chapter 6 Methods of Using Internal and External Clock Function

6.1 Internal Clock Function of AD

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the AD conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSource = USB5953 _CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means AD work frequency is 100000Hz (that is, 100 KHz, 10uS/point).

6.2 External Clock Function of AD

External Clock Function refers to the use of the outside clock signals to trigger the AD conversion regularly. The clock signals are provide by the CLKIN pin of P5. The outside clock can be provided by USB5953 clock output (CLKOUT of P5), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSource = USB5953_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the AD is fully controlled by the external clock frequency.

6.3 Methods of Using AD Continuum and Grouping Sampling Function

6.3.1 AD Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of AD, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the parameters ADPara.ADMode = USB5953_ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the AD converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

6.3.2 AD Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two groups, this period of time is known as the Inter-group Spacing. Cycles of Group refers to numbers of the cycle acquisition for each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycles. The conversion process of this acquisition mode as follows: a

short time stop after the channels conversion in the group (that is, Inter-group Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer inter-group interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, the cycles of a group depends on ADPara. Loops of Group and the inter-group interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, group cycles and inter-group interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle ≥ internal clock sampling cycle × the total number of sampling channels × cycles of Group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period × the total number of sample channels × group cycles + AD chips conversion time + inter-group interval
External signal cycle = (cycle signal points / group cycles) × Group cycle
External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)
Group Cycle = external clock cycle
External signal cycle = (cycle signal points / group cycles) × group cycle
External signal frequency = 1 / external signal cycle

Formula Notes:
The internal sampling clock cycle = 1 / (AD Para. Frequency)
The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1
Cycles of Group = AD Para. Loops of Group
AD Chips conversion time = see "AD Analog Input Function" parameter
Inter-group interval = AD Para. Group Interval
Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10uS), cycles of group is 1, inter-group interval (Group Interval) = 50uS, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10uS to sample the two data, 20uS to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50uS group interval ends. We start the next group,

begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

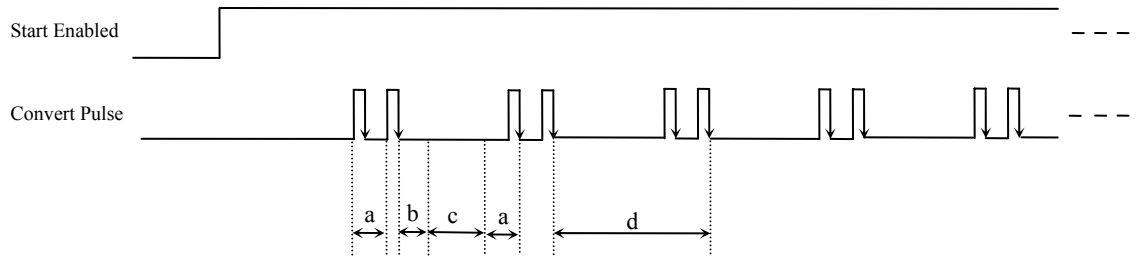


Figure 6.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle
b— AD chips conversion time
c— inter-group interval
d— group cycle

Change the group cycles into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10uS to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50uS group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

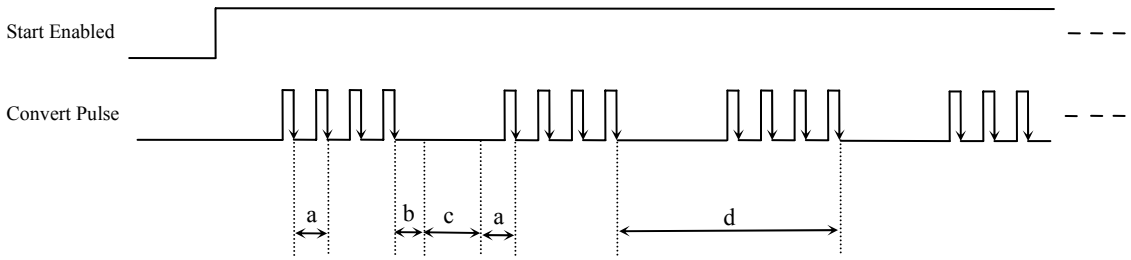


Figure 6. 2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Note: a— internal clock sample cycle
b— AD chips conversion time
c— inter-group interval
d— group cycle

Chapter 7 Timer/Counter Function

Mode 0: Interrupt on terminal count

In this mode, when the initial value assigned, if GATE is high level, the counter immediately to count by subtracting 1, and the OUT becomes low level. When the value decremented to 1, OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. GATE=1 enables counting; GATE=0 disables counting.

Time diagram is shown in Figure 1.

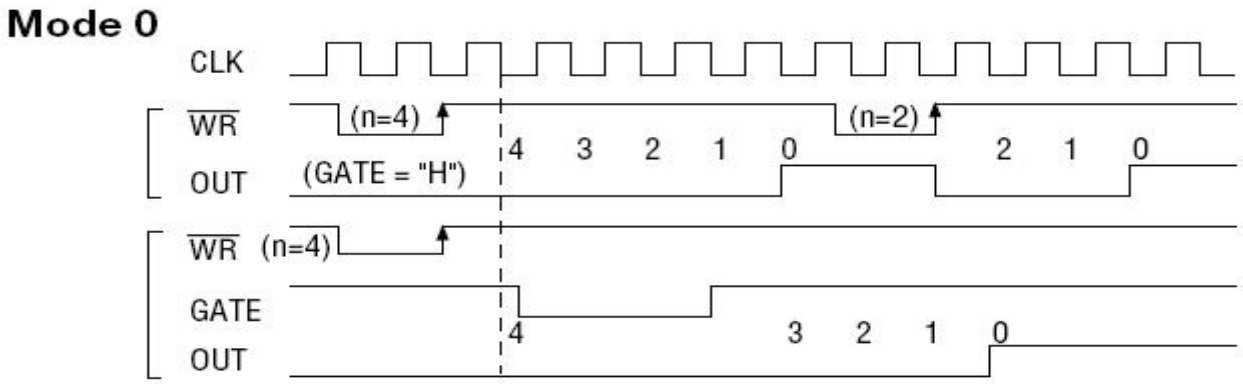


Figure 1

Mode 1: Hardware retriggerable ONE-SHOT

The mode can work under the role of GATE of gating signal. When given the initial value, OUT becomes high level, if GATE has a rising edge, the counter immediately begins to count, at this time the output OUT turns into low level. When the count ends, in other word, the count value turns to 0, the output OUT turns to high level, the output width of one-shot is deceived by initial value. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “0” and there is a “GATE” rising edge, the counter will begin to count from the new value. If there is a “GATE” rising edge when the counter is working, the current counting is stopped and re-start counting from the initial value. So the output single pulse has been widened

Time diagram is shown in Figure 2.

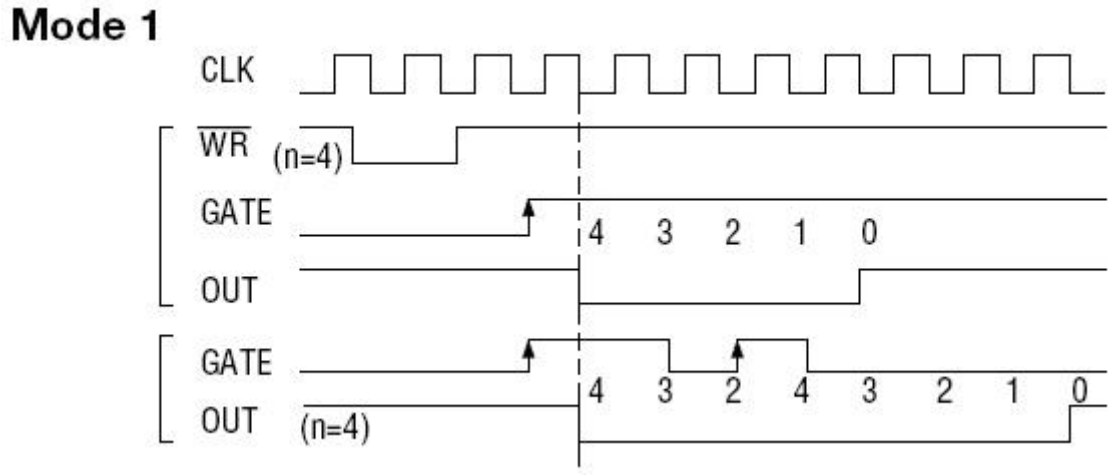


Figure 2

Mode 2: Rate Generator

Set this mode, the counter loads the initial value of n, start counting from the (n-1), OUT becomes high level, when the count value reaches 0, the OUT becomes low level. After a CLK cycle, OUT restore high level, and then the counter automatically load the initial value n, restart counting from the (n-1). Therefore, the output terminal will continue to output negative pulse, whose width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. Set a new initial value during a counting period, the counter start a new count cycle next time. GATE=1 enables counting; GATE=0 disables counting.

Time diagram is shown in Figure 3.

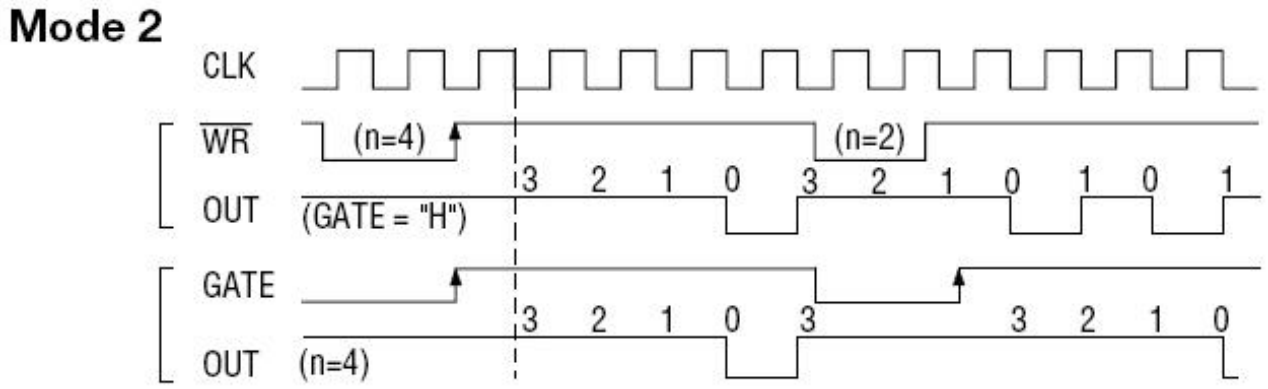


Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter loads the initial value of n, start counting from the (n-1) when the signal of GATE has a rising edge, timer/counter begins to count by subtracting “1” each time. The “OUT” terminal output high level when the count value is more than half of the initial count value, and it turn to low level when the count value is less than half of the initial value. If the initial count value n is an even number, then output 1:1 square wave, if the initial count value a is odd number, the output has remained high level during the previous (n +1)/2 count period, but the output becomes low level during the post (n-1) /2 count period, that is high level has one clock cycle than low level. Set a new initial value during a counting period, the counter start a new count cycle next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted.

Time diagram is shown in Figure 4.

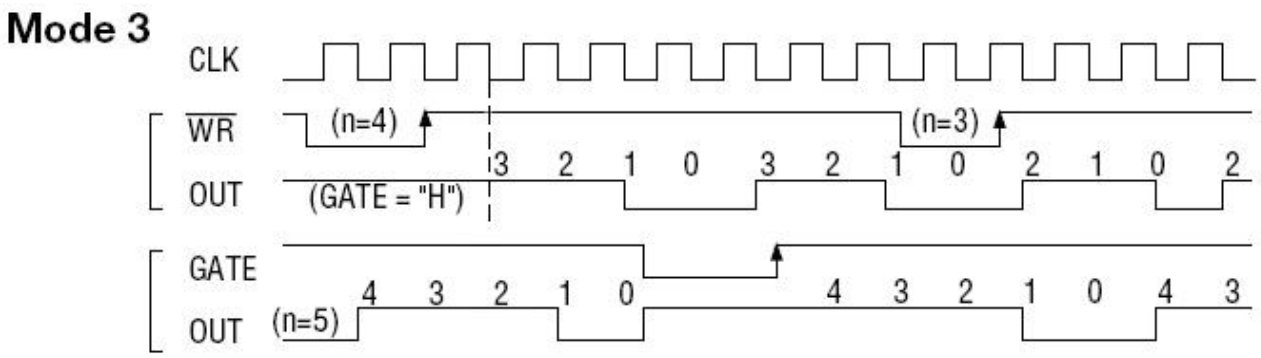


Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter starts counting after is given the initial value n, and OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting.
Time diagram is shown in figure 5.

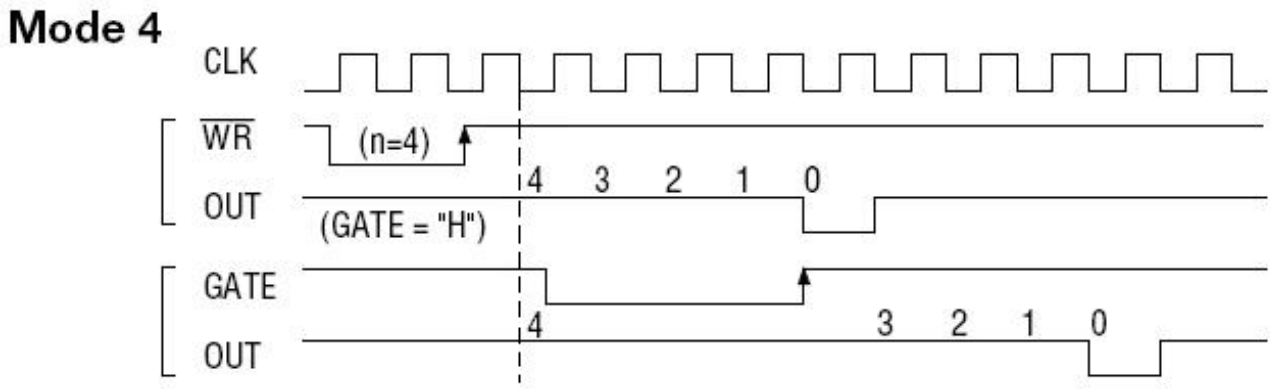


Figure 5

Mode 5: Hardware triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “0” and there is a “GATE” rising edge, the counter will begin to count from the new value.
Time diagram is shown in figure 6.

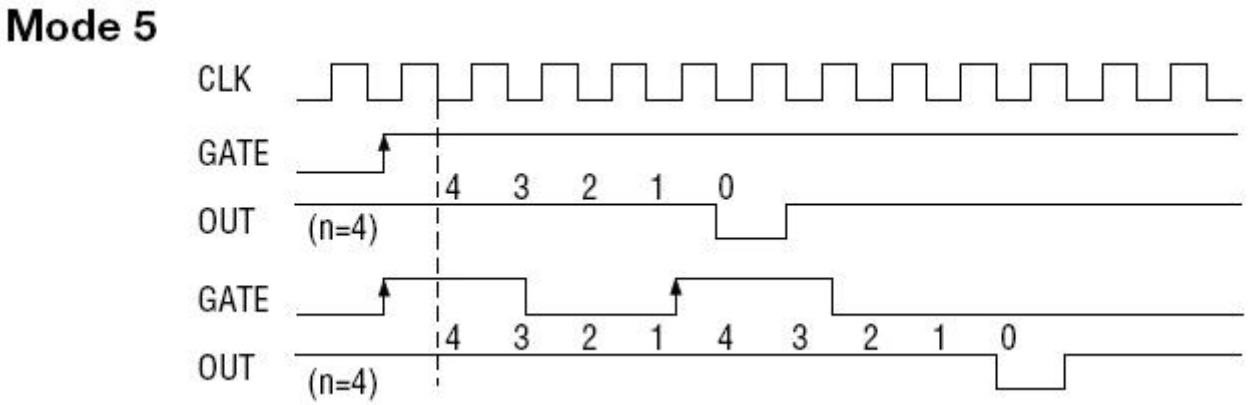


Figure 6

Chapter 8 Notes, Calibration and Warranty Policy

8.1 Notes

In our products' packing, user can find a user manual, a USB5953 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB5953, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB5953 module.

8.2 Analog Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. In the manual, we introduce how to calibrate USB5953 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB5953 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9999.69mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 9999.69mV or about 9999.69mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

8.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate USB5953 in ±5V input range; calibrations of other output ranges are similar.

1）Connect the ground of the digital voltage meter to any AGND. Connect the input side of the voltage meter to the DA input channel which needs calibration. Run USB5953 test procedure under Windows, select the DA output detection.

2) Set the analog value to 2048. Then adjust potentiometer RP7 to make the output of AO0~AO3 are 0.000V. Adjust potentiometer RP3 to make the outputs of AO0~AO3 0.000V.

3）Set the analog value to 4095. Adjust potentiometer RP3 to make the output of AO0 is 4997.55mV.

4）Repeat steps above until meet the requirement.

8.4 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.